HIGH-SPEED DATA BUFFER

ABSTRACT

Disclosed is a high-speed data buffer, wherein a buffer circuit composed of a ring counter is divided into two sampling circuits composed of a rising-edge portion and a falling-edge portion, and both of the two sampling circuits comprises a trigger circuit and a sampling clock generation circuit. In such a manner, the excess pulse edge can be ensured to occur before the correct edge so that the error data caused by the excess pulse can be over-written with the correct data input afterwards. Therefore, a clock cycle of timing margin can be obtained and the data stored in the data buffer can be ensured to be correct.